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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,342	02/07/2002	Krishna B. Rajan	5858P7100	4281

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,342	RAJAN, KRISHNA B.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-33 have been examined. Claims 1-4, 14-17, 21, and 23-26 have been amended.

2. The claims objections and rejections under 35 U.S.C 112 second paragraph have been overcome by the Applicant's amendment and, therefore, withdrawn by the Examiner.

Response to Arguments

3. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 14-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US-2003/0115522), hereinafter Nadeau-Dostie, in view of Muradali et al. (US-6587981), hereinafter Muradali.

Claims 1, 14, 21 and 23:

Nadeau-Dostie teaches hierarchical circuit 10 which includes a top-level hierarchical block 12 (TOP), two embedded hierarchical functional blocks 14 and 16 (plurality of embedded logic test (ELT) blocks), a boundary scan register 18 (periphery flops), a Test Access Port (TAP) 20, and a test controller 22. FIG. 15 is a state diagram of a TAP according to the IEEE 1149.1 standard. (Page 2, ¶ 28). Nadeau-Dostie also teaches that memory elements located at the periphery or boundary of a logic block are referred to as "peripheral memory elements" where the boundary scan register chain 18 can be used as a peripheral chain (periphery flops). Nadeau-Dostie further teaches block 62 includes a multiplexer 82, for selectively connecting the serial input of peripheral segment 76 to one of two sources including the output of internal segment 78 of block 62 or to the serial output of internal segment 72 of parent block 60. (Page 3 and 4, ¶ 31, 33 and 37). Nadeau-Dostie discloses that the chain segments of a block are arranged on a scan path which originates from or includes a block serial input by connecting a segment serial input to a block input, to the serial output of another segment in the block or to the serial output of a segment located in an embedded block one level down in design hierarchy and by connecting the block serial input of embedded blocks to the block serial input (selecting a single chain of all ELT blocks and inserting the scan chain into the TOP scan chain). Nadeau-Dostie also discloses that electronic files stored on a computer readable storage medium describe the scan paths of the block and the scan paths of embedded blocks and allows for pattern generation (machine readable medium that provides instructions per claim 23). (Page 3, ¶ 35). Nadeau-Dostie does not explicitly teach "identifying scan-in and scan-out ports of periphery flops of ELT blocks"

and "bypassing the scan-in and scan-out ports of the periphery flops of the ELT blocks". However, Nadeau-Dostie does teach input and output peripheral memory elements which receive and output signals from embedded logic blocks. (Page 3, ¶ 31). Muradali teaches the ASIC chip 100 as an example has two main cores which are an A core 102 and a B core 104 where the B core 104 has two sub-cores, B.1 sub core 106 and B.2 sub-core 108 (ELT blocks). Muradali also teaches for testing purposes, each section has connections for scanning in test data or information and for scanning out test results or information which are referred to as scan-in (SI) and scan-out (SO) ports and terminals. Muradali further teaches the level of integration of a core is a measure of the number of parents it possesses in the hierarchy (identifying scan-in and scan-out ports of periphery flops of ELT blocks). Muradali discloses in order to provide a path for test data to flow, a scan test wrapper cell element, or wrapper cell 214, is attached to the core 200. Muradali also discloses a wrapper is a single cell or a chain of cells connected to the inputs and outputs of a core 200 which used to isolate a core from the rest of an integrated circuit during scan testing (bypassing the scan-in and scan-out ports of the periphery flops of the ELT blocks). (Col. 3, l. 43 – Col. 4, l. 58). Muradali further discloses configurations of the "wrapper cell" in Fig. 9 and 10. It would have been obvious to one of ordinary skill in the art at the time the invention was made modify Nadeau-Dostie's testing method to incorporate Muradali's integration method of the embedded core blocks. It also would have been obvious to one of ordinary skill in the art at the time the invention was made modify Nadeau-Dostie's input and output peripheral memory elements with Muradali wrapper cell 214. The artisan would have

been motivated to do so because this would enable Nadeau-Dostie to identify and selectively bypass the scan-in (SI) and scan-out (SO) ports of the embedded cores which where known to be correct in design and performance, consequently shorting test time and freeing up valuable test resources.

Claims 2, 15 and 24:

Nadeau-Dostie teaches blocks 14 and 16 are embedded in the top-level block and, thus, are located one level down in design hierarchy (division is performed in a substantially hierarchical manner). Two hierarchical blocks are shown for illustration purposes only. It is to be understood that the circuit may have any arbitrary number of hierarchical blocks and levels. (Page 2, ¶ 28).

Claims 3, 16 and 25:

Nadeau-Dostie teaches input peripheral memory elements are configurable in "internal test mode" in which data contained in the peripheral memory element is passed on to the internal circuitry of the block. Nadeau-Dostie also teaches that the control signals C1 and C2 of multiplexer 82 are set to 0,0 to perform a scan test of top level block 60. (Page 3, ¶ 32 and Page 4, ¶ 42).

Claims 4, 17 and 26:

Nadeau-Dostie teaches a Test Access Port (TAP) 20, and a test controller 22. FIG. 15 is a state diagram of a TAP according to the IEEE 1149.1 standard. (Page 2, ¶ 28).

Claims 5:

Nadeau-Dostie teaches that the circuit is placed in test mode (step 100) by applying an appropriate instruction to the chip (TAP). In response, the test controller generates an appropriate Mode signal whereby the serial input of each block is connected to its predetermined circuit primary serial input, and the serial input of each block scan chain is connected to the block serial input. This establishes a scan path to all scannable memory elements in all blocks in the circuit (chip single scan chain mode). (Page 5, ¶ 55).

Claims 6:

Nadeau-Dostie teaches a Test Access Port (TAP) 20, and a test controller 22. FIG. 15 is a state diagram of a TAP according to the IEEE 1149.1 standard. (Page 2, ¶ 28).

Claims 7, 18, 22 and 27:

Nadeau-Dostie further teaches block 62 includes a multiplexer 82, for selectively connecting the serial input of peripheral segment 76 (bypassing periphery flops) to one of two sources including the output of internal segment 78 of block 62 or to the serial output of internal segment 72 of parent block 60. Nadeau-Dostie also teaches multiplexer 92 receives the serial output of peripheral segment 78 in parent block 62 and the output of internal segment 86 and applies its output to peripheral segment 90 (plurality of multiplexers). (Page 4, ¶ 37 and 38).

Claims 8, 19 and 28:

Nadeau-Dostie teaches input peripheral memory elements are configurable in "internal test mode" in which data contained in the peripheral memory element is

passed on to the internal circuitry of the block. Nadeau-Dostie also teaches that the control signals C1 and C2 of multiplexer 82 are set to 0,0 to perform a scan test of top level block 60. (Page 3, ¶ 32 and Page 4, ¶ 42).

Claims 9, 20 and 29:

Nadeau-Dostie teaches a Test Access Port (TAP) 20, and a test controller 22. FIG. 15 is a state diagram of a TAP according to the IEEE 1149.1 standard. (Page 2, ¶ 28).

5. Claims 10, 11, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US-2003/0115522), hereinafter Nadeau-Dostie, in view of Muradali et al. (US-6587981), hereinafter Muradali, in further view of Sato et al. (US-2001/0022743), hereinafter Sato.

Claims 10, 11, 30 and 31:

Nadeau-Dostie does not explicitly teach "plurality of blocks within a test access port (TAP) block, per claims 10 and 30, that comprise of a device identity chain block and a bypass block, per claims 11 and 31". However, Nadeau-Dostie does teach a Test Access Port (TAP) 20, and a test controller 22 and illustrates in FIG. 15, a state diagram of a TAP according to the IEEE 1149.1 standard. (Page 2, ¶ 28). Sato teaches the TAP is an interface and control circuit for a scan test and a BIST circuit which are defined by the IEEE 1149.1 standard. Sato also teaches the TAP is constituted by a bypass register 211 to be used for shifting test data from an input port to an output port; a data register 212 to be used for transmitting a specific signal to the circuit; a device ID

register 213 for setting a manufacturing identification number peculiar to a chip; an instruction register 214 to be used when a data register is to be selected and an internal test method is to be controlled; a controller 215 for controlling the whole TAP circuit (a plurality of blocks (claims 10 and 30) and a device identity chain block and a bypass block, claims 11 and 31. (Page 8, ¶ 99, Fig. 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie's TAP block 20 with Sato's TAP 200 to include the plurality of blocks, namely the bypass register 211 and the device ID register 213, for example. The artisan would have been motivated to do so because this would enable Nadeau-Dostie's TAP block 20 to shifting test data from an input port to an output port and set a manufacturing identification number peculiar to a chip.

6. Claims 12, 13, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US-2003/0115522), hereinafter Nadeau-Dostie, in view of Muradali et al. (US-6587981), hereinafter Muradali, in further view of Kim et al. (US-5504756), hereinafter Kim.

Claims 12 and 32:

Nadeau-Dostie does not explicitly teach "re-circulating data back to a scan chain to restore the pre-scandump state of the chip after a scandump". However, Nadeau-Dostie does teach in Fig. 15, that the TAP controller is in the "Capture-DR" and "Shift-DR" TAP states which is well known in the art to be the last mode is where a particular TAP instruction is loaded into the TAP instruction register and results in the internal F/F

clocks being clocked in phase with the TCK input pin and is used to scan initialize or scandump. Kim illustrates the recirculating of data in a scan chain in Fig. 3. Kim also discloses The module 300 includes a series of flip-flops FF0 302, FF1 304, FF2 306, FF3 308 and FF4 310 that are connected by a feedback loop from the output of the last flip-flop 302 to the input of multiplexer 314 for selecting as an input to the scan chain either an external scan input SI or the feedback input SO running from the output of the last flip-flop 302 in the chain (re-circulating data back to a scan chain). (Col. 4, lines 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie's scan chain configuration to in Figure 3, for example, to adopt Kim's feedback loop to connect the output of scan chain 88 to the input 68 of mutiplexer 82. The artisan would have been motivated to do so because this would enable Nadeau-Dostie's scan chain configuration to re-circulating data back to a scan chain to restore the pre-scandump state of the chip after a scandump

Claims 13 and 33:

Nadeau-Dostie teaches a multiplexer 82 for performing the re-circulation of data. (Fig. 3).

Conclusion

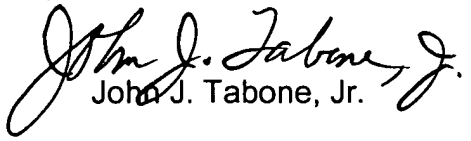
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John J. Tabone, Jr.

Examiner
Art Unit 2133

Guy J. Lamarre
Primary Examiner